REMARKS

Claims 1, 3, 5-8, 10, 12-15, 17 and 19-21 are pending in the present application. Claims 1, 3, 5, 8, 10, 12, 15, 17 and 19 have been amended. Claims 4, 11 and 18 have been canceled.

Claim Rejections – 35 U.S.C. 102

Claims 1, 3, 5, 6, 8, 10, 12, 13, 15, 17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Brunolli et al. reference (U.S. Patent No. 6,201,491). Claim 1 has been amended to include the features of dependent claim 4, claim 8 to include the features of dependent claim 11, and claim 15 to include the features of dependent claim 18. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

Claim Rejections – 35 U.S.C. 103

Claims 4, 11 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

As noted above, claim 1 has been amended to include the features of dependent claim 4, as including in combination a first switching circuit "having a plurality of P-channel type MOS transistors each of which is connected directly to the first potential, and to respective ones of the first connecting points and the first node"; and a second

switching circuit "having a plurality of N-channel type MOS transistors each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node". As further featured, the control circuit controls the P-channel type MOS transistors and the N-channel type MOS transistors. Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious the digital-to-analog converting circuit of claim 1 for at least the following reasons.

The Examiner has acknowledged that the Brunolli et al. reference does not disclose first switches that are P-channel type MOS transistors and second switches that are N-channel type MOS transistors. In order to overcome this acknowledged deficiency of the Brunolli et al. reference, the Examiner has asserted that P-MOS and N-MOS transistors are known to be active devices capable of switching components or elements in a circuitry, and that it is known that transistors are used as an alternative way to switch elements in a system. The Examiner has alleged that it would have been obvious "that Brunolli et al. would perform the same function as the claimed invention". Applicant respectfully disagrees for the following reasons.

As described beginning on page 2, line 3 of the present application, switches SW0 to SW7 of the conventional D/A converting circuit 40 as illustrated in Fig. 4 of the present application, are generally implemented as analog switches shown in Fig. 5. The analog switches as shown in Fig. 5 are a combination of P-channel type MOS transistors and N-channel type MOS transistors, so that ON resistances of switches

SW0 to SW7 can be closer to a constant value.

However, as further described beginning on page 2, line 20 of the present application with reference to Fig. 6C, the composite resistance of ON resistances of conventional analog switches SW0 to SW7 configured as in Fig. 5 of the present application, are not completely constant and depend on the input side potential. As a result, D/A conversion of such conventional circuits is imprecise. Moreover, due to the ON resistances and parasitic capacitance within the circuit using the above noted conventional analog switches, conversion speed is poor.

In a preferred embodiment as described beginning on page 12, line 7 of the present application, the PMOS transistors P1 to P7 as illustrated in Fig. 1 are used for switching paths between the reference potential terminal Vref and the reference potential side resistors R1. Accordingly, all of the potentials to be applied to the PMOS transistors P1 to P7 are the reference potential, and are common. Thus, the composite resistances of ON resistances are all constant for the PMOS transistors. The same is true with respect to the NMOS transistors N0 to N7 (ground potential side switches). As a result, the precision of D/A conversion is improved.

Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or even remotely suggest a first switching circuit having a plurality of P-channel type MOS transistors, and a second switching circuit having a plurality of N-channel type MOS transistors. The Brunolli et al. reference as relied upon by the Examiner does not particularly specify what type of transistors are used as respective

switches $S_9 - S_{12}$ in the potentiometer of Fig. 3, and/or what specific type transistors are used as respective switches $S_1 - S_4$. The prior art as relied upon would thus provide no motivation as to why all of switches $S_9 - S_{12}$ should be P-channel type MOS transistors, and all of switches $S_1 - S_4$ should be N-channel type MOS transistors. The Examiner has thus failed to establish why one of ordinary skill would be motivated to provide switches $S_9 - S_{12}$ of the Brunolli et al. reference as PMOS transistors and switches $S_1 - S_4$ as NMOS switches, as opposed to providing all of switches $S_9 - S_{12}$ and $S_1 - S_4$ as PMOS transistors or all of switches $S_9 - S_{12}$ and $S_1 - S_4$ as NMOS transistors. Regardless of whether P-MOS and N-MOS transistors are known to be active devices capable of switching components or elements in circuitry, the Examiner has failed to establish the necessary motivation to modify the circuit in Fig. 3 of the Brunolli et al. reference to use respective P-channel type MOS transistors and respective N-channel type MOS transistors, as would be necessary to meet the features of claim 1. Accordingly, Applicant respectfully submits that the digital-to-analog converting circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1, 3, 5 and 6, is improper for at least these reasons.

The digital-to-analog converting circuit of claim 8 has been amended to include the features of dependent claim 11, as including a plurality of P-channel type MOS transistors and a plurality of N-channel type MOS transistors. Applicant respectfully submits that the Examiner has failed to establish the necessary motivation to modify the

circuit in Fig. 3 of the Brunolli et al. reference so that each of switches $S_9 - S_{12}$ are P-channel type MOS transistors, and each of switches $S_1 - S_4$ are as N-channel type MOS transistors. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 8 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 8, 10, 12 and 13, is improper for at least these reasons.

Claim 15 has been amended to include the features of dependent claim 18, as including a plurality of P-channel type MOS transistors and a plurality of N-channel type MOS transistors. Applicant respectfully submits that the digital-to-analog converting circuit of claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 15, 17, 19 and 20, is improper for at least somewhat similar reasons as set forth above with respect to claim 8.

Claims 7, 14, and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference in view of the Leung et al. reference (U.S. Patent No. 6,400,300). Applicant respectfully submits that the Leung et al. reference as secondarily relied upon by the Examiner does not overcome the above noted deficiencies of the primarily relied upon Brunolli et al. reference, and that this rejection is improper for at least these reasons.

Conclusion

Since independent claims 1, 8 and 15 have been amended merely to include the features of respective dependent claims 4, 11 and 18, this amendment should not be construed as raising new issues that would require further consideration and/or search. Consideration and entry of this Amendment thus should not be an undue burden, because the scope of claims 1, 8 and 15 has already been examined in view of claims 4, 11 and 18. **The Examiner is thus respectfully urged to enter this Amendment.**

Applicant further respectfully requests the Examiner to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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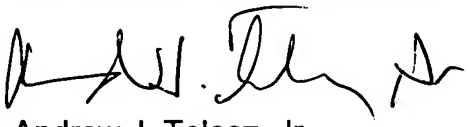

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